REMARKS

Claims 1, 3 and 5-11 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claims 1, 3, and 5-9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Akimoto et al. (U.S. Pat. No. 6,856,308 B2). This rejection is respectfully traversed.

Claim 1 recites a display driver for driving data lines of an electro optic device based on display data. The display driver comprises a display data random access memory including a plurality of word lines, a plurality of column lines, and a plurality of memory cells each storing display data of one pixel. The display driver also comprises a display address decoder selecting a word line of the display data random access memory based on a display address and a display column address decoder selecting a column line of the display data random access memory based on a display column address. The display driver also comprises a plurality of read-out bit lines each commonly coupled to a memory cell group specified by a corresponding column line. The display driver also comprises a scroll bus coupled to the plurality of read-out bit lines and a plurality of shift register latches outputting a plurality of shift outputs shifted based on a given shift clock. The display driver also comprises a plurality of data latches, each of which corresponds to one of the data lines. The plurality of data latches load display data on the scroll bus. One of the plurality of the data latches is

coupled to one of the plurality of shift register latches. The display driver also comprises a driving circuit driving the data lines based on the display data loaded in the plurality of data latches. Display data of one pixel being is read out from a memory cell specified by a word line selected by the display address decoder and a column line selected by the display column address decoder. The display data of one pixel is output to the scroll bus via the read-out bit line coupled to the memory cell. The display data of one pixel on the scroll bus is loaded in one of the plurality of data latches. The display data of one pixel is shifted from the scroll bus for storing in the plurality of data latches. One of the plurality of data latches loads display data of one pixel on the scroll bus based on one of the plurality of shift outputs. Akimoto et al fails to teach or suggest the display driver recited by Claim 1.

In Akimoto et al., a gate line shift register (shown as 4 in Figure 1) is connected to a gate line, not a data line of the display. Akimoto et al., Col. 4, Lines 10-11. As stated in Akimoto et al., "[t]he gate of the pixel switch 2 is connected to gate line shift register 4 through a gate line 3." Akimoto et al., Col. 4, Lines 10-11. In this way, the gate line shift register of Akimoto et al. does not provide a shift clock to a data latch.

In the display driver of Claim 1, on the other hand, a plurality of shift register latches output a plurality of shift outputs shifted based on a given shift clock. Further, in the display driver of Claim 1, a plurality of data latches, each of which correspond to one of the data lines, load display data on a scroll bus and one of the plurality of data latches is coupled to one of the plurality of shift register latches. Further, in the display driver of Claim 1, one of the plurality of data latches loads display data of one pixel on

the scroll bus based on one of the plurality of shift outputs. Akimoto et al. is silent as to at least these features of the display driver of Claim 1.

For at least these reasons, Akimoto et al. fails to teach or suggest each and every element recited by Claim 1. With respect to Claims 3 and 5-7, each depends either directly or indirectly from Claim 1 which defines over Akimoto et al., as discussed in detail above. Claim 8 recites limitations similar to those discussed above with respect to Claim 1 and likewise defines over Akimoto et al. Claim 9 depends from Claim 8 and likewise defines over Akimoto et al. Reconsideration and withdrawal of the rejections are respectfully requested.

REJECTION UNDER 35 U.S.C. § 103

Claims 10 and 11 stand rejected under 35 U.S.C. § 103(a) in view of Akimoto et al. (U.S. Pat. No. 6,856,308 B2) and Oka et al. (U.S. Pat. No. 4,600,200). This rejection is respectfully traversed.

Claims 10 and 11 depend from Claims 1 and 8 respectively, which define over the prior art as discussed in detail above. For at least the above reasons, Claims 10 and 11 likewise define over the prior art. Reconsideration and withdrawal of the rejections are respectfully requested.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is

believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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